

HIGH OUTPUT HIGH EFFICIENCY LOW VOLTAGE CHARGE PUMP

Field of the Invention

5 The present invention relates generally to semiconductor integrated circuits. More particularly, it pertains to charge pumps.

Background of the Invention

System designs are routinely constrained by a limited number of readily
10 available power supply voltages (V_{cc}). For example, consider a portable computer system powered by a conventional battery having a limited power supply voltage. For proper operation, different components of the system, such as display, processor, and memory components employ diverse technologies which require power to be supplied at various operating voltages. Components often require
15 operating voltages of a greater magnitude than the power supply voltage and, in other cases, a voltage of reverse polarity. The design of a system, therefore, includes power conversion circuitry to efficiently develop the required operating voltages. One such power conversion circuit is known as a charge pump. Charge pumps have been used as on-chip voltage generators capable of providing a voltage
20 more positive than the most positive external supply or more negative than the most negative external supply. The demand for highly efficient and reliable charge pump circuits has increased with the increasing number of applications utilizing battery powered systems, such as notebook computers, portable telephones, security devices, battery-backed data storage devices remote controls, instrumentation, and
25 patient monitors, to name a few.

Inefficiencies in conventional charge pumps lead to reduced system capability and lower system performance in both battery and non-battery operated systems. Inefficiency can adversely affect system capabilities e.g., limited battery life, excess heat generation and high operating costs. Examples of lower system
30 performance include low speed operation, excessive operating delays, loss of data,

limited communication range, and inability to operate over wide variations in ambient conditions including ambient light level and temperature.

In addition to constraints on the number of power supply voltages available for system design, there is increasing demand for reducing magnitudes of the power supply voltages due to shrinking die size and also to save power. The demand in
5 diverse application areas requires highly efficient charge pumps that operate from a supply voltage of around one volt.

Thus, there is a need for a low voltage charge pump that can operate at supply voltages less than one volt while reducing the die area and increasing the
10 power efficiency.

Summary of the Invention

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in
15 part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims and their equivalents.

20 Other aspects of the invention will be apparent on reading the following detailed description of the invention and viewing the drawings that form a part thereof.

The charge pump of the present invention provides, among other things, a high output high efficiency low voltage charge pump. According to one
25 embodiment, it has two staggered phase generators which act together with a delay to produce non-overlapping signals required to drive charge and precharge capacitors to work around a supply voltage of 1.0 Volts (V_{cc}), to provide a higher output voltage and superior current per unit area.

Sub C1 30 An illustrative embodiment includes a charge pump circuit. The charge pump circuit includes an oscillator to generate an oscillating signal. The charge

Brief Description of the Drawings

In the drawings, like numerals describe substantially similar components throughout the several views. Like numerals having different letter suffixes represent different instances of substantially similar components.

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Figure 1 is a block diagram illustrating generally one embodiment of an integrated circuit of the present invention.

Figure 2 is a block diagram illustrating generally one embodiment of a charge pump of the present invention.

10 Figure 3A is a timing diagram illustrating generally one embodiment of a first and second phase signals that are non-overlapping and crossing around their high points during a phase cycle.

 Figure 3B is a timing diagram illustrating generally one embodiment of a first and second phase signals that are non-overlapping and crossing around their
15 low points during a phase cycle.

Figure 4 is a schematic diagram illustrating generally one embodiment of a charge pump circuit of the present invention.

Figure 5 is a flow chart illustrating one embodiment of the working of charge pump circuit of the present invention.

20 Figures 6A and 6B are timing diagrams illustrating generally one embodiment of signals generated at various node points when the supply voltage (V_{cc}) is around 1.0 volts.

 Figures 7A and 7B are timing diagrams illustrating generally another embodiment of signals generated at various node points when the supply voltage
25 (V_{cc}) is around 1.5 volts.

 Figures 8A and 8B are timing diagrams illustrating generally another embodiment of signals generated at various node points when the supply voltage (V_{cc}) is around 2.3 volts.

Figure 9 is an elevation view of a substrate containing semiconductor dies.

30 Figure 10 is a block diagram of an exemplary circuit module.

Figure 11 is a block diagram of an exemplary memory module.

Figure 12 is a block diagram of an exemplary electronic system.

Figure 13 is a block diagram of an exemplary memory system.

Figure 14 is a block diagram of an exemplary computer system.

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Description of the Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced.

- 10 These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural changes may be made without departing from the scope of the present invention. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of the present invention is defined by
- 15 the appended claims and their equivalents.

- 20 The transistors described herein include transistors from bipolar-junction technology (BJT), field effect technology (FET), or complimentary metal-oxide-semiconductor (CMOS). A metal-oxide-semiconductor (MOS) transistor includes a gate, a first node (drain) and a second node (source). Since a MOS transistor is typically a symmetrical device, the true designation of "source" and "drain" is only possible once voltage is impressed on the terminals. The designations of source and drain herein should be interpreted, therefore, in the broadest sense.

- 25 The charge pump circuit here described is a two phase circuit, therefore only one half of the charge pump is producing V_{ccp} at any given time. The "first phase" is herein defined as the time when output IN1 is high and the "second phase" is defined as the time when the output IN2 is high.

The terms "crossing around their high points" and "high-high crossing points" refers to the crossing of the first and second signals around their high points of the signals generated by the first and second primary phase generators. Also the

phases for the first and second main pump capacitors generally cross high-high for optimum efficiency of the charge pump.

The term "phase generator" means an oscillator to generate a first phase and a second phase during a phase cycle.

5 The terms "crossing around their low points" and "low-low crossing points" refers to the crossing of the first and second signals around low points of the signals generated by the first and second primary phase generators. Also the phases for the precharge caps generally cross low-low for optimum efficiency of the charge pump.

10 The term "pre-charging capacitors/device" described herein includes any devices capable of providing charges to maintain a predetermined level of charges in an energy-storing device while a system that includes the energy-storing device is turned off. The reason for pre-charging is thus: the energy-storing device may have to store a large amount of charges to enable a charge pump circuit to provide a
15 high-voltage signal. Without pre-charging, an undesired amount of time may have to be taken once the system is turned on to charge the energy-storing device. The pre-charging device described herein can be a square-law device. The pre-charging device described herein can be any transistor fabricated on an integrated circuit using any fabrication technique. The pre-charging device described herein
20 however, may be fabricated as an n-channel transistor with its drain and gate connected together; the drain is connected to an external supply.

25 The terms "pre-boot capacitors" and "pre-booting stages" described herein includes any devices capable of providing charges to maintain a predetermined level of charges in an energy storing device while a system that includes the energy-storing device is turned off. Pre-boot capacitors are used first to boot the first and second main pump capacitors to a predetermined boot level. While the first main capacitor is outputting a charge in the first phase, the pre-boot is booting the second main capacitor to a predetermined boot level in the second phase and vice-versa. This process hides the pre-boot time and enables the charge pump

circuit to run at a faster cycle time resulting in outputting more charge for a given size of a capacitor.

The term "booting" described herein refers to the principle that the charge on a capacitor cannot change instantaneously. This is, if the voltage on a first side
5 of capacitor is instantaneously increased, the second side of the capacitor will increase by the same amount. The voltage on the second side of the capacitor is therefore "booted" higher.

The term "main energy storing device" means the main pump capacitor that outputs a desired level of a high-voltage signal during the first or second phase of a
10 phase cycle.

The embodiments of the present invention generate higher voltage at a high efficiency by a charge pump using a low voltage supply.

Figure 1 is a block diagram of a device illustrating generally one embodiment of the present invention. The device 100 has a charge pump 102, an
15 oscillator 110, and operational circuit 104. The operational circuit 104 can be any functional circuit; for example, a memory device such as a dynamic random access memory (DRAM) or flash memory. The charge pump 102 converts V_{cc} provided by an external power supply into a higher potential V_{ccp} . The operational circuit 104, therefore, has both V_{cc} and V_{ccp} available.

Figure 2 is a block diagram of a two phase charge pump circuit 102
20 illustrating generally one embodiment of the present invention. The charge pump circuit 102 includes a plurality of phase generators. The plurality of phase generators further including first and second primary phase generators 210A and 210B which receive an oscillating signal from an oscillator 110, and generates a
25 first and a second phase signal having a high-high crossing point, and a third and a fourth phase signal having a low-low signal crossing point.

In one embodiment, at node 260, a capacitor may be placed upon the node 260 to ground for noise filtering. However, in other embodiments, linear, non-linear, or a combination of linear and non-linear elements may be placed upon the
30 node 260 to function as an output load.

and 210B respectively, that are non-overlapping and crossing around high points 315 during every phase cycle. Also shown are the sixth and fifth phase signals 330 and 340 generated by the first and second secondary phase generators 220A and 220B respectively, that is similar to the first and second phase signals, and
5 including a pre-determined delay 't' from the first and second phase signals respectively.

Figure 3B is a timing diagram illustrating generally by way of example but not by way of limitation one embodiment of portion of third and fourth phase signals 350 and 360 generated by the first and second primary phase generators
10 210A and 210B respectively, that are non-overlapping and crossing around low points 335 during every phase cycle.

Figure 4 is a schematic diagram illustrating generally by way of example but not by way of limitation one embodiment of a charge pump circuit. In this embodiment, the charge pump circuit 102 includes first and second primary phase
15 generators 210A and 210B, first and second secondary phase generators 220A and 220B, first and second pre-boot capacitors and associated precharge circuits 230A and 230B, first and second main pump capacitors and associated precharge circuits 240A and 240B, and a first and a second p-channel and associated circuitry 250A and 250B. The charge pump is designed symmetrically such that during a first
20 phase the charge pump provides a pump voltage V_{ccp} using one-half of the charge pump circuit and during the second phase V_{ccp} is provided using the other-half of the charge pump circuit. The operation of the charge pump is described in detail below following a description of the charge pump circuit.

The first and second primary phase generators 210 and 210B have an
25 oscillating input POSC, which receives an oscillating signal produced by oscillator 110 located in the integrated circuit 100. Inverter 402 and muxes 404 and 406 provide signals IN1 and IN2 which are 180 degrees out of phase with a crossing point very near $V_{cc}/2$. IN1 and IN2 are the inputs to the cross-coupled NAND gates 408 and 410. The cross-coupled NAND gates and subsequent invertors 412, 416,
30 420, 414, 418 and 422 provide third and fourth signals that are non-overlapping

and crossing around low points of their signals during the first and second phases at node point E and F respectively. Subsequently invertors 424 and 426 provide first and second phase signals that are non-overlapping and crossing around high points of their signals during the first and second phases at nodes A and B respectively.

5 The first and second phase signals coming from nodes A and B drive the first and second secondary phase generators 220A and 220B. The first and second secondary phase generators 220A and 220B generate fifth and sixth phase signals at nodes C and D, which are delayed from the first and second phase signals. Driving the first and second secondary phase generators 220A and 220B with an
10 output of the first and second primary phase generators 210A and 210B provides an inherent delay through NAND gates 436 and 438, and further driving through invertors 440, 444, 448, 452, 442, 446, 450, and 453 of the first and second primary phase generators 210A and 210B. In one embodiment delays 432 and 434 can be
15 added to provide additional delay to output the first and sixth phase signals for supply voltages operating above 1.5 volts. Delays 432 and 434 can be removed for supply voltages operating below 1.5 Volts. The fifth and sixth phase signals are similar to first and second phase signals, and only they have a predetermined delay from the first and second phase signals. This delay sets the amount of time necessary for pre-booting the first and second main capacitors 240A and 240B.

20 The first and second phase signals coming from nodes A and B also drive the first and second pre-boot capacitors 462 and 464 respectively. Whereas the third and fourth phase signals coming from nodes E and F drive the first and second pre-boot pre-charge capacitors 474 and 476 respectively. First and second pre-boot pre-charge capacitors 474 and 476 are responsible for recharging the first
25 and second pre-boot capacitors 462 and 464. The first and second pre-boot pre-charge capacitors 474 and 476 are tied in a cross-coupled manner, such that they precharge each other through n-channel gates 478 and 480. The reason for third and fourth phase signals to be non-overlapping and crossing each other around their low points is that the gate of the first pre-boot precharge capacitor 474 should close
30 low before the gate of second pre-boot precharge capacitor 476 goes high,

otherwise the boost voltage of the second pre-boot precharge capacitor 476 would leak off through the precharge transistor 480. The gate nodes of these first and second pre-boot precharge capacitors 474 and 476 also drive the precharge transistors 468 and 469 of the pre-boot capacitors 462 and 464 respectively. Also the gate nodes of the first and second pre-boot precharge capacitors drive charge sharing transistors 465 and 471 which provide the path that charge shares the first and second pre-boot capacitors 462 and 464, to a first and second main pump capacitors 486 and 492 of a first and second main pump capacitor and associated pre-charge circuitry 240A and 240B to a pre-determined boot level. Diode transistors 467, 468, 469, 470, 479, and 481 are there for power-up. They charge-up first and second pre-boot capacitors 462 and 464, and first and second pre-boot precharge capacitors 474 and 476 at power-up, so that they can start pumping. Diode transistors 472 and 466 clamp gates of the first and second pre-boot precharge capacitors 474 and 476 to an n-channel VT above the gates of the first and second main pump capacitors 486 and 492 respectively. This helps to limit over-voltage and puts the excess charge onto the main pump cap where it can be passed to V_{ccp} .

The first and second secondary phase generators 220A and 220B work just like the first and second primary phase generators 210A and 210B except they get their input from the first and primary phase generators 210A and 210B instead of the POSC input received by the first and second primary phase generators 210A and 210B. The outputs of the first and second secondary phase generators are at nodes C and D (fifth and sixth phase signals). The outputs of signals at the first and second secondary phase generators 220A and 220B at nodes C and D (fifth and sixth phase signals) are similar to the outputs of signals at the nodes A and B (first and second phase signals), except they are delayed by the first and second secondary phase generators by a pre-determined delay. Again the fifth and sixth phase signals are non-overlapping and crossing around high points of their signals. Fifth and sixth phase signals coming from the first and second secondary phase generators 220A and 220B drive the first and second main pump capacitors 486

and 492 to a third pre-determined level respectively. Fifth and sixth signals are non-overlapping and crossing around high points because the signals at gate nodes of the first and main pump capacitors K and L cross around high points. The signals at nodes K and L needs to cross around high points, because they drive first and second p-channel circuitry 250A and 250B, which pass the charge from the first and second main capacitors 486 and 492 to V_{ccp} . Another reason it is desirable to have the fifth and sixth signals cross around high points, is that only one of the gates of the first and second p-channel circuitry 403 and 405 is on at any one time. This is because, any amount of time that both p-channel gates 403 and 405 are on, will rob charge from the V_{ccp} by passing it back to the first and second main pump capacitors 486 and 492, which are trying to precharge. Nodes I and J cross at a low-low point similar to the nodes E and F that drive them through precharge capacitors 474 and 476. Nodes I and J precharge the preboot capacitors 462 and 464 to a full V_{cc} potential through the precharge gates 468 and 469.

15 The diode transistors 494, 496, 499, and 500 of the first and second main pump capacitor and associated circuitry 240A and 240B are for power-up. These diode transistors 494, 496, 499, and 500 provide a starting voltage to the first and second main pump precharge capacitors 488 and 490. Transistor 497 precharges the second main pump precharge capacitor 490, and transistor 495 precharges the first main pump precharge capacitor 488. The first and second main pump precharge capacitors 490 and 488 are used to precharge the first and second main pump capacitors 486 and 492 to a second pre-determined level through precharge devices 493 and 498. The seventh and eighth phase signals coming from nodes G and H are supplied by AND-INVERTs 417, 423, 419, and 425 of nodes from the first and second primary and secondary phase generators 210A, 210B, 220A and 220B respectively. The fifth and sixth phase signals from nodes G and H are small instead of the half cycle, because these signals should not be recharging the first and second main pump capacitors 486 and 492 while they are being pre-booted by the first and second pre-boot capacitors 462 and 464, otherwise the pre-boot charges will be shunted to V_{cc} .

In one embodiment the charge pump circuitry 102 enables to pre-boot one main pump capacitor while the other main pump capacitor is outputting the charge. This further enables to hide the preboot time, which in-turn enables the pump to run at a faster cycle time and hence a higher output charge. Also in this

5 embodiment the charge pump circuitry 102 including staggered phase generators operating without a delay element at voltages lower than 1.5 Volts, with the pre-boot capacitors 486 and 492 adding a head room at voltages less than 1.5 Volts, and with the p-channel circuitry 250A and 250B giving an operating head room of about 800 millivolts, enables the charge pump circuitry to operate efficiently at

10 supply voltages around 1.0 Volts.

Figure 5 is a flow diagram illustrating one embodiment of the working of a charge pump circuit of the present invention. The first step in the method of operating the charge pump is to generate an oscillating signal 510. In one

15 embodiment the oscillating signal is input to a primary phase generator for generating first and second phase signals that are non-overlapping and crossing each other around their highest points during a phase cycle from the oscillating signal 510. Then the primary phase generator further generates third and fourth phase signals that are non-overlapping and crossing each other around their lowest points during each phase cycle from the oscillating signals 510. Then the primary

20 phase generator further generates seventh and eighth phase signals. Then a secondary phase generator receives the first and second phase signals from the primary phase generator and generates a fifth and sixth phase signals similar to the first and second phase signals and having a pre-determined delay from the first and second phase signals. Then a first preboot capacitor and associated driving

25 circuitry receives the first and third phase signals from the primary phase generator during the first phase, and preboots a first main pump to a first predetermined level during a first phase 520A. A second preboot capacitor and associated driving circuitry receives the second and fourth phase signals from primary phase generator during the second phase, and preboots a second main pump to a first predetermined

30 level during the second phase 520B. A first main pump precharge capacitor

receives the seventh phase signal from the primary phase generator, and the first main pump is further precharged by first main pump precharge capacitor during second phase to a second predetermined level 530B. A second main pump precharge capacitor receives the eighth phase signal from the primary phase generator, and the second main pump is further precharged by second main pump precharge capacitor during first phase to a second predetermined level 530A. Then in one embodiment the fifth phase signal from the secondary phase generator is input to raise the first main pump to a third predetermined level 530A and a charge is output from the first main pump during the first phase 540A. Then in this embodiment the sixth phase signal from the secondary phase generator is input to raise the second main pump to a third predetermined level 530B and a charge is output from the second main pump during the second phase 540B. The charge from the first main pump passes through the pass gate 1 (p-channel circuitry 1) to provide a pump voltage V_{ccp} during the first phase 550, and the charge from the second main pump passes through the pass gate 2 (p-channel circuitry 2) to provide the pump voltage V_{ccp} during the second phase 550. The charge pump is designed symmetrically, such that during a first phase the pump provides a pump voltage V_{ccp} using one-half of the pump circuit and during the second phase V_{ccp} is provided using the other-half of the circuit. This process repeats itself for every charge cycle and generally hides the preboot time required to pre-boot the first and second main capacitors 240A and 240B. As a result, the charge pump circuitry 102 can run at a faster cycle time resulting in outputting more charge for a given size of a capacitor.

Figures 6A and 6B are timing diagrams illustrating generally one embodiment of signals at various node points when a supply voltage (V_{cc}) is around 1.0 volts. Timing diagrams 610A and 610B show first and second phase signals generated by a primary phase generator that are non-overlapping and crossing around their high points at nodes A and B during first and second phases. Timing diagrams 620A and 620B show fifth and sixth phase signals generated by a secondary phase generator (at nodes C and D) that are similar to the first and

second phase signals, that are delayed from the first and second phase signals. Timing diagrams 630A and 630B show seventh and eighth phase signals generated by the primary phase generator (at nodes G and H) that are smaller instead of a half cycle, because these signals should not be recharging first and second main pump capacitors 486 and 492 while they are being pre-booted by first and second pre-boot capacitors 462 and 464, otherwise the pre-boot charges will be shunted to V_{cc} . Timing diagrams 640A and 640B show third and fourth signals generated by the primary phase generator (at nodes E and F), that are non over-lapping and crossing around their low points during the first and second phases. Timing diagrams 650A and 650B show that signals at nodes I and J cross around low points, similar to the signals at nodes E and F, that drive them through precharge capacitors 474 and 476. Also the signals at nodes I and J precharge the preboot capacitors 462 and 464 to a full V_{cc} potential through precharge gates 468 and 469. Timing diagrams 660A and 660B show that the signals at nodes K and L cross around their high points, because they drive the p-channel circuitry 250A and 250B, which pass the final charge from the first and second main pump capacitors 486 and 492 to V_{ccp} . Figures 6A and 6B generally illustrate one embodiment of the present invention outputting a higher voltage (V_{ccp}) of around 2.0 volts when the supply voltage (V_{cc}) is around 1.0 volts.

Figures 7A and 7B are similar to Figures 6A and 6B, except for the present invention outputting a higher voltage (V_{ccp}) of around 3.0 volts when the supply voltage (V_{cc}) is around 1.5 volts.

Figures 8A and 8B are similar to Figures 6A and 6B, except for present invention outputting a higher voltage (V_{ccp}) of around 4.0 volts when the supply voltage (V_{cc}) is around 2.3 volts.

With reference to Figure 9, in one embodiment, a semiconductor die 710 is produced from a silicon wafer 700. A die is an individual pattern, typically rectangular, on a substrate that contains circuitry to perform a specific function. A semiconductor wafer will typically contain a repeated pattern of such dies containing the same functionality. Die 710 may contain circuitry for the inventive

memory device, as discussed above. Die 710 may further contain additional circuitry to extend to such complex devices as a monolithic processor with multiple functionality. Die 710 is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die for unilateral or bilateral communication and control.

As shown in Figure 10, two or more dies 710 may be combined, with or without protective casing, into a circuit module 800 to enhance or extend the functionality of an individual die 710. Circuit module 800 may be a combination of dies 710 representing a variety of functions, or a combination of dies 710 containing the same functionality. Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules and may include multi-layer, multi-chip modules. Circuit module 800 may be a sub-component of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft and others. Circuit module 800 will have a variety of leads 810 extending therefrom providing unilateral or bilateral communication and control.

Figure 11 shows one embodiment of a circuit module as memory module 900. Memory module 900 generally depicts a Single In-line Memory Module (SIMM) or Dual In-line Memory Module (DIAM). A SIMM or DIAM is generally a printed circuit board (PCB) or other support containing a series of memory devices. While a SIMM will have a single in-line set of contacts or leads, a DIAM will have a set of leads on each side of the support with each set representing separate I/O signals. Memory module 900 contains multiple memory devices 910 contained on support 915, the number depending upon the desired bus width and the desire for parity. Memory module 900 may contain memory devices 910 on both sides of support 915. Memory module 900 accepts a command signal from an external controller (not shown) on a command link 920 and provides for data input and data output on data links 930. The command link 920 and data links 930 are

connected to leads 940 extending from the support 915. Leads 940 are shown for conceptual purposes and are not limited to the positions shown in Figure 7.

Figure 12 shows an electronic system 1000 containing one or more circuit modules 800. Electronic system 1000 generally contains a user interface 1010.

5 User interface 1010 provides a user of the electronic system 1000 with some form of control or observation of the results of the electronic system 1000. Some examples of user interface 1010 include the keyboard, pointing device, monitor and printer of a personal computer; the tuning dial, display and speakers of a radio; the ignition switch and gas pedal of an automobile; and the card reader, keypad,
10 display and currency dispenser of an automated teller machine. User interface 1010 may further describe access ports provided to electronic system 1000. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules 800 may be a processor providing some form of manipulation, control or direction of inputs
15 from or outputs to user interface 1010, or of other information either preprogrammed into, or otherwise provided to, electronic system 1000. As will be apparent from the lists of examples previously given, electronic system 1000 will often contain certain mechanical components (not shown) in addition to circuit modules 800 and user interface 1010. It will be appreciated that the one or more
20 circuit modules 800 in electronic system 1000 can be replaced by a single integrated circuit. Furthermore, electronic system 1000 may be a sub-component of a larger electronic system.

Figure 13 shows one embodiment of an electronic system as memory system 1100. Memory system 1100 contains one or more memory modules 900
25 and a memory controller 1110. Memory controller 1110 provides and controls a bidirectional interface between memory system 1100 and an external system bus 1120. Memory system 1100 accepts a command signal from the external bus 1120 and relays it to the one or more memory modules 900 on a command link 1130. Memory system 1100 provides for data input and data output between the one or
30 more memory modules 900 and external system bus 1120 on data links 1140.

Figure 14 shows a further embodiment of an electronic system as a computer system 1200. Computer system 1200 contains a processor 1210 and a memory system 1100 housed in a computer unit 1205. Computer system 1200 is but one example of an electronic system containing another electronic system, i.e. memory system 1100, as a sub-component. Computer system 1200 optionally contains user interface components. Depicted in Figure 10 are a keyboard 1220, a pointing device 1230, a monitor 1240, a printer 1250 and a bulk storage device 1260. It will be appreciated that other components are often associated with computer system 1200 such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that the processor 1210 and memory system 1100 of computer system 1200 can be incorporated on a single integrated circuit. Such single package processing units reduce the communication time between the processor and the memory circuit.

Conclusion

A low voltage two-phase charge pump is described which produces a V_{ccp} voltage of up to or greater than $2 V_{cc}$. The charge pump can operate at supply voltages of around 1 volt (V_{cc}). The head room of conventional charge pumps is overcome while reducing the power requirement and die area of other low voltage charge pumps. The charge pump uses two phase generators, delay elements, pre-boot capacitors, and requires only two main pump capacitors which are used 50% of the time. This is a substantial improvement over four-phase charge pumps which use 4 main pump capacitors that are active only 25% of the time. Also the two phase generators, which act together with a delay to produce the non-overlapping signals required to drive the charge and precharge capacitors to output the charge from one main capacitor in one phase and pre-boot the other main pump capacitor in the second phase, thereby hiding the pre-boot time and increasing the charge pump cycle time, which results in higher output for a given size of capacitor.

